Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): An integrated circuit package comprising:

an integrated circuit die, said integrated circuit die having a top side and a bottom side opposite said top side, said top side including at least one bond pad;

at least one raised interconnect located over and conductively coupled to said at least one bond pad; and

a **single-layer** solid flexible dielectric circuit film having a top surface, a bottom surface and a routing conductor, the flexible circuit film having at least one outer landing formed on the top surface and at least one inner landing formed on the bottom surface such that the landings on the top and bottom surfaces are fully supported by the circuit film, wherein the outer landing is laterally offset from the inner landing and the two landings are connected via the routing conductor, which extends laterally within the **single-layer** solid flexible dielectric circuit film,

wherein the flexible circuit film being located over and conductively attached to at least one raised interconnect such that an air gap is formed between said integrated circuit die and said flexible circuit film.

2. (original): The integrated circuit package of claim 1 wherein said air gap has a height in the range of between about 10μm to 500μm.

3. (original): The integrated circuit package of claim 1 wherein said flexible circuit film is substantially the same size as said integrated circuit die.

4. (canceled)

5. (previously presented): The integrated circuit package of claim 1 wherein said outer landing is offset a horizontal distance from said inner landing, and further wherein said horizontal distance in the range of between about 50μm to 1,000μm.

6. (previously presented): The integrated circuit package of claim 1 further comprising at least one contact bump conductively coupled with said outer landing of said flexible circuit film.

7. (original): The integrated circuit package of claim 1 further comprising an under bump pad formed over said bond pad and conductively coupled to said at least one bond pad and said at least one raised interconnect.

8-14. (canceled)

15. (currently amended): An integrated circuit wafer having a top side and a bottom side opposite said top side, said integrated circuit wafer comprising:

a plurality of integrated circuit dice, said plurality of integrated circuit dice having a plurality of bond pads located on said top side of said integrated circuit wafer;

a plurality of raised interconnects formed over and conductively coupled to said plurality of bond pads; and

a **single-layer** solid flexible dielectric circuit film having a top surface, a bottom surface and routing conductors, the flexible circuit film having a plurality of outer landings located on the top surface and a plurality of inner landings located on the bottom surface such that the landings on the top and bottom surfaces are fully supported by the circuit film, wherein the individual outer landings are laterally offset from the individual inner landings and the landings are connected via routing conductors, which extend laterally within the **single-layer** solid flexible dielectric circuit film,

wherein the flexible circuit film being located over and conductively attached to the plurality of raised interconnects such that an air gap is formed between said integrated circuit wafer and said flexible circuit film.

16. (original): The integrated circuit wafer of claim 15 wherein said air gap has a height in the range of between about 10μm to 500μm.

17. (original): The integrated circuit wafer of claim 15 wherein said integrated circuit wafer further comprises a plurality of under bump pads formed over and conductively coupled to each of said plurality of bond pads.

18. (canceled)

19. (previously presented): The integrated circuit wafer of claim 15 wherein each of said plurality of outer landings are offset a horizontal distance from a corresponding one of said inner landings, and further wherein said horizontal distance is in the range of between about 50μm to 1,000μm.

20. (previously presented): The integrated circuit wafer of claim 15 further comprising a plurality of contact bumps formed on and conductively coupled with said outer landings of said flexible circuit film.

21. (previously presented): An integrated circuit package as recited in claim 1 wherein the flexible dielectric circuit film is made up of multiple layers.

22. (previously presented): An integrated circuit package as recited in claim 1 wherein the flexible dielectric circuit film contains at least one outer landing connected to at least one inner landing via a routing connector in such a way as to form a cantilever-like structure.

23-24. (canceled)

25. (previously presented): An integrated circuit wafer as recited in claim 15 wherein the flexible dielectric film is made up of multiple layers.

26. (previously presented): An integrated circuit wafer as recited in claim 15 wherein the flexible dielectric circuit film contains a plurality of outer landings connected to a plurality of inner landings via routing connectors in such a way as to form a plurality of cantilever-like structures.

27-28. (canceled)

29. (previously presented): The integrated circuit package of claim 1, wherein the laterally extended segment of the routing conductor is necessarily required to connect the two landings.

30. (previously presented): The integrated circuit package of claim 29, wherein the routing conductor is formed into a step-like shape.

31. (previously presented): The integrated circuit package of claim 30, wherein the routing conductor connects to the outer landing with a first vertical segment and connects to the inner landing with a second vertical segment, wherein the first and second vertical segments are laterally offset from each other, the first and second vertical segments being necessarily connected together with the laterally extended segment of the routing conductor.

32. (previously presented): The integrated circuit wafer of claim 15, wherein the laterally extended segments of the routing conductors are necessarily required to connect the landings.

33. (previously presented) The integrated circuit wafer of claim 32, wherein the routing conductors are formed into a step-like shape.

34. (previously presented): The integrated circuit wafer of claim 33, wherein the routing conductors connect to the outer landings with a plurality of first vertical segments and connect to the inner landings with a plurality of second vertical segments, wherein each of the first and second vertical segments are laterally offset from each other, each of the first and second vertical segments being necessarily connected together with the laterally extended segments of the routing conductor.